WHAT IS CLAIMED IS:

1. A signal-processing circuit comprising:

a phase locked loop circuit for receiving playback data obtained as a result of analog-to-digital conversion of a playback signal from a first equalization circuit;

wherein said first equalization circuit is composed of a transversal filter.

2. A signal-processing circuit according to claim 1, wherein said first equalization circuit is subjected to adaptive equalization.

3. A signal-processing circuit according to claim 1, further comprising a second equalization circuit provided on the downstream side from said phase locked loop circuit;

wherein a sampling frequency of said first equalization circuit is made approximately equal to a channel clock frequency;

a next time transfer characteristic of said first equalization circuit is made equal to a product of a present time transfer characteristic of said first equalization circuit and a present time transfer characteristic of said second equalization circuit; and

a next time transfer characteristic of said second equalization circuit is flattened.

4. A signal-processing circuit according to claim 3, wherein a transversal filter is used for each of said first equalization circuit and said second equalization circuit, to obtain the next time transfer characteristic of said first equalization circuit by setting a next time tap coefficient of said first equalization circuit to a result of convolutional integration of a present time tap coefficient of said first equalization circuit and a present time tap coefficient of said second equalization circuit.

5. A signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on the downstream side from said phase locked loop circuit;

wherein said first equalization circuit is subjected to adaptive equalization by applying tap-coefficient-updating information output by said adaptive equalization circuit to a tap coefficient of said first equalization circuit in accordance with the following equation:

next time k-th tap coefficient = present time k-th tap coefficient + k-th tap-coefficient-updating information

6. A signal-processing circuit according to claim

1, further comprising a second equalization circuit provided on the downstream side from said phase locked loop circuit;

wherein a sampling frequency of said first equalization circuit is set at a value higher than a channel clock frequency;

the next time transfer characteristic of said first equalization circuit is divided into a portion in a frequency band "a" being within a frequency band of said second equalization circuit and a portion in a frequency band "b" being out of a frequency band of said second equalization circuit;

the portion of the next time transfer characteristic of said first equalization circuit in the frequency band "a" is taken as a product of a portion of the present time transfer characteristic of said first equalization circuit in the frequency band "a" and the present transfer characteristic of said second equalization circuit, and the portion of the next time transfer characteristic of said first equalization circuit in the frequency band "b" is set to zero; and

the next time transfer characteristic of said second equalization circuit is flattened.

7. A signal-processing circuit according to claim

6, wherein a transversal filter is used for each of said first and second equalization circuits, to determine the next time tap coefficient of said first equalization circuit by a manner of:

obtaining a tap coefficient A of said first equalization circuit by subjecting the present time tap coefficient of said first equalization circuit to fc/S1 thinning, where S1 denotes a sampling frequency of said first equalization circuit and fc denotes a channel lock frequency,

obtaining a convolution-integration result C in accordance with an equation of C = A * B, where symbol * denotes a convolution-integration operator and B denotes the present time tap coefficient of said second equalization circuit,

obtaining a tap coefficient D by subjecting said convolution-integration result C to S1/fc-times interpolation, and

taking the tape coefficient D as the next time tap coefficient of said first equalization circuit.

8. A signal-processing circuit according to claim 6, wherein a transversal filter is used for each of said first and second equalization circuits, to determine the next time tap coefficient of said first equalization

circuit by a manner of:

obtaining a tap coefficient B of said second equalization circuit by subjecting the present time tap coefficient of said second equalization circuit to fc/S1 thinning, where S1 denotes a sampling frequency of said first equalization circuit and fc denotes a channel lock frequency,

obtaining a convolution-integration result C in accordance with an equation of C = A * B, where symbol * denotes a convolution-integration operator and A denotes the present time tap coefficient of said first equalization circuit, and

taking the convolution-integration result C as the next time tap coefficient of said first equalization circuit.

9. A signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on the downstream side from said phase locked loop circuit;

wherein said first equalization circuit is subjected to adaptive equalization by a manner of:

making a sampling frequency S1 of said first equalization circuit higher than a channel clock frequency fc;

obtaining a tap coefficient A by subjecting the present time tap coefficient of said first equalization circuit to fc/S1 thinning;

calculating a next time value of said tap coefficient A in accordance with the following equation:

next time k-th value of tap coefficient A = present time k-th value of tap coefficient A + k-th tap-coefficient-updating information

obtaining a tap coefficient B by subjecting said next time value of said tap coefficient A to S1/fc-times interpolation; and

setting said tap coefficient B to a next time tap coefficient of said first equalization circuit.

10. A signal-processing circuit comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal; and

a digital phase locked loop circuit for receiving said digital signal from said analog-to-digital converter;

wherein said digital signal output by said analog-to-digital converter is supplied to said digital phase locked loop circuit so as to fetch a detection-point voltage.

11. A signal-processing circuit according to claim 10, further comprising a first equalization circuit provided between said analog-to-digital converter and said phase locked loop circuit;

wherein said first equalization circuit is composed of a digital transversal filter.

12. A signal-processing circuit according to claim 11, further comprising an interpolation circuit provided between said first equalization circuit and said digital phase locked loop circuit;

wherein said interpolation circuit is adapted to interpolate sparse pieces of sampling data with a period close to a channel-clock period.

13. A signal-processing circuit according to claim 12, wherein a sampling frequency of said analog-to-digital converter is about equal to a channel-clock frequency.

14. A signal-processing circuit according to claim 12, wherein said interpolation circuit includes a transversal filter for interpolation and an R-times interpolation circuit; and

data is thinned at intervals of R taps of said transversal filter for interpolation.

15. A signal-processing circuit according to claim

14, wherein said R-times interpolation circuit is composed of R pieces of transversal filters disposed in parallel to each other.

16. A signal-processing circuit according to claim 12, wherein said interpolation circuit includes a low-magnification interpolation circuit composed of a transversal filter and a Q-times linear interpolation circuit provided on the downstream side from said low-magnification interpolation circuit.

17. A signal-processing circuit according to claim 16, wherein said Q-times linear interpolation circuit is composed of Q pieces of interpolation circuits disposed in parallel to each other.

18. A signal-processing circuit according to claim 12, wherein said phase locked loop circuit includes:

a data selector for receiving $R \times Q$ parallel trains of $S \times R \times Q$-times interpolation data from said interpolation circuit and selecting 0 or 1 piece of data closest to a detection point from said parallel data for $S > 1$;

a detection point computing circuit for controlling said data selector; and

a circuit for reporting 0 or 1 detection point.

19. A signal-processing circuit according to claim

12, wherein said phase locked loop circuit includes:

a data selector for receiving R × Q parallel trains of S × R × Q-times interpolation data from said interpolation circuit and selecting 0, 1, or 2 pieces of data closest to detection points from said parallel data for S ≦ 1;

a detection point computing circuit for controlling said data selector; and

a circuit for reporting 0, 1 or 2 detection points.

20. A signal-processing circuit according to claim 12, wherein said phase locked loop circuit includes:

data selectors of the number of Dmax for receiving P × R × Q parallel trains of S × R × Q-times interpolation data from said interpolation circuit and selecting the number of data closest to the maximum detection points from said parallel data;

detection point computing circuits for controlling one of said data selectors of the number of Dmax; and

a circuit for reporting the number of detection points.

21. A signal-processing circuit according to claim 11, wherein said phase locked loop circuit includes:

a thinning period correcting means for absorbing frequency deviations while being updated in accordance

with an equation given below:

$$d = d \pm \Delta d,$$

where d denotes a thinning period, and Δd denotes a thinning period correction quantity;

wherein the value of the thinning period correction quantity Δd given to said thinning period correcting means is changed in accordance with a response speed.

22. A signal-processing circuit according to claim 11, wherein a buffer memory in which data output by said phase locked loop circuit is stored and from which data is read with another clock signal, is provided on the downstream side from said phase locked loop circuit.

23. A signal-processing circuit according to claim 22, wherein said buffer memory has two memory banks; and

for $S \leqq 1$, odd numbered detection point data and even numbered detection point data, which are output by said phase locked loop circuit, are stored alternately into said two memory banks of said buffer memory.

24. A signal-processing circuit according to claim 22, wherein said buffer memory has memory banks of the number of Dmax, where Dmax is a maximum number of detection points simultaneously output by said phase locked loop circuit for receiving $P \times R \times Q$ parallel trains of $S \times R \times Q$-times interpolation data, and is

expressed by an equation of Dmax = Int (P/S) + 1; and

letting the number of detection points reported by said phase locked loop circuit be D (D $\leqq$ Dmax), the detection point data output by said phase locked loop circuit are stored in said buffer memory having said D banks.

25. A signal-processing circuit according to claim 22, wherein the frequency of said clock signal for reading data from said buffer memory is higher than the frequency of a channel clock signal.

26. A signal-processing circuit according to claim 25, wherein said buffer memory includes:

an empty-buffer detection circuit for outputting an empty-data signal to indicate that said buffer memory is empty;

wherein an operation of circuits provided at the back of said empty-buffer detection circuit is stopped on the basis of said empty-data signal.

27. A signal-processing circuit according to claim 22, further comprising a voltage controlled oscillator for generating said clock signal for reading data from said buffer memory.

28. A signal-processing circuit according to claim 27, wherein an oscillation frequency of said voltage

controlled oscillator is controlled so that neither empty-data state nor data overflow occurs in said buffer memory.

29. A signal-processing circuit according to claim 28, wherein said voltage controlled oscillator is subjected to feedback control so that a read address to read out data from said buffer memory and a write address to write data into said buffer memory satisfy the following equation:

(write address - read address) = a maximum difference

30. A recording and playback apparatus having a recording system and a playback system each employing a signal-processing circuit, said signal-processing circuit employed in said playback system comprising:

a first equalization circuit;

a phase locked loop circuit for receiving playback data obtained as a result of analog-to-digital conversion of a playback signal from said first equalization circuit; and

a second equalization circuit provided on the downstream side from said phase locked loop circuit;

wherein each of said first and second equalization circuits is composed of a transversal filter;

a sampling frequency of said first equalization circuit is set at a value approximately equal to a channel clock frequency;

a next time transfer characteristic of said first equalization circuit is made equal to a product of a present time transfer characteristic of said first equalization circuit and a present time transfer characteristic of said second equalization circuit; and

a next time transfer characteristic of said second equalization circuit is flattened.

31. A recording and playback apparatus including a recording system and a playback system each employing a signal-processing circuit, said signal-processing circuit employed in said playback system comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal;

a digital phase locked loop circuit for receiving said digital signal from said analog-to-digital converter;

a first equalization circuit composed of a digital transversal filter, said first equalization circuit being provided between said analog-to-digital converter and said phase locked loop circuit; and

an interpolation circuit for interpolating sparse pieces of sampling data with a period close to a channel clock period, said interpolation circuit being provided between said first equalization circuit and said digital phase locked loop circuit;

wherein said interpolation circuit includes a Q-times linear interpolation circuit and an R-times interpolation circuit composed of transversal filters of the number of R.

a sampling frequency of said ADC is set at a value approximately equal to a channel clock frequency; and

said digital signal output by said analog-to-digital converter is supplied to said digital phase locked loop circuit so as to fetch a detection point voltage.